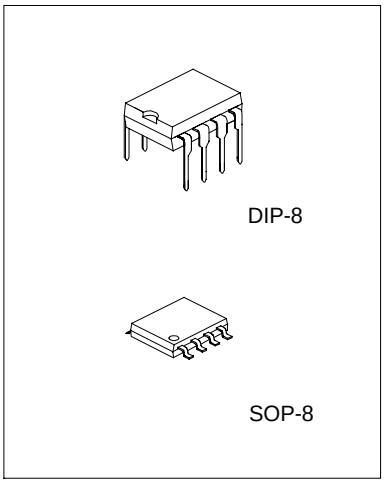
DUAL OPERATIONAL AMPLIFIER



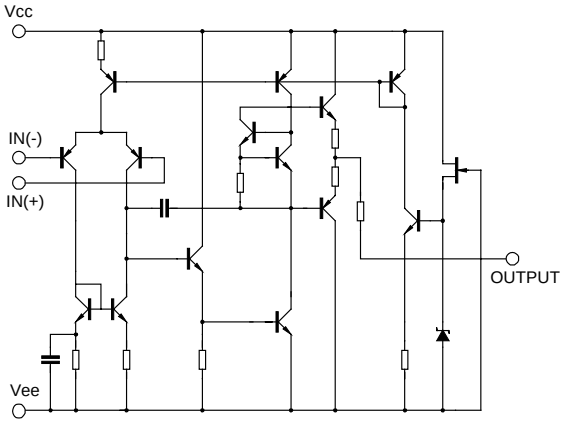
DESCRIPTION

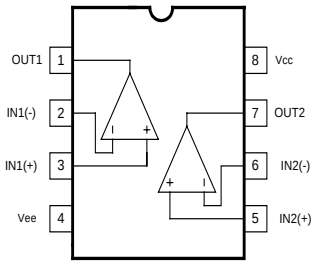
The JRC4558 is a monolithic integrated circuit designed for dual operational amplifier.

FEATURES

*No frequency compensation required.
*No latch-up
*Large commom mode and differential voltage range
*Parameter tracking over temperature range
*Gain and phase match between amplifiers
*Internally frequency compensated
*Low noise input transistors

BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	Vcc	± 16	V
Differential input voltage	$V_{I(DIFF)}$	±16	V
Power Dissipation	P_D	400	mW
Input Voltage	V_I	±15	V
Operating Temperature	T_{OPR}	0~+70	°C
Storage Temperature	T_{STG}	-65~+150	°C

ELECTRICAL CHARACTERISTICS(Ta=25°C ,Vcc=15V,Vee=-15V)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Supply Current	Icc			3.5	5.6	mA
Input offset voltage	V_{IO}	Rs<10kΩ		2	6	mV
Input offset current	I_{IO}			5	200	nA
Input bias current	I_{BIAS}			30	500	nA
Large signal voltage gain	Gv	Vo(p-p)=10V,R_L<2kΩ	20	200		V/mV
Commom Mode Input Voltage Range	$V_{I(R)}$		±12	±13		V
Commom Mode Rejection Ratio	CMRR	Rs<10kΩ	70	90		dB
Supply Voltage Rejection Ratio	PSRR	Rs<10kΩ	76	90		dB
Output Voltage swing	Vo(p-p)	R_L>10kΩ		±12	±14	V
Power Comsumption	Pc			70	170	mV
Slew Rate	SR	Vi=10V,R_L>2kΩ,C_L<100pF	1.2			V/μs
Rise Time	T_{RIS}	Vi=20mV,R_L>2kΩ, C_L<100pF		0.3		μs
Overshoot	OS	Vi=20mV,R_L>2kΩ,C_L<100pF		15		%

TYPICAL PERFORMANCE CHARACTERISTICS

Fig.1 Positive output voltage swing vs Load resistance

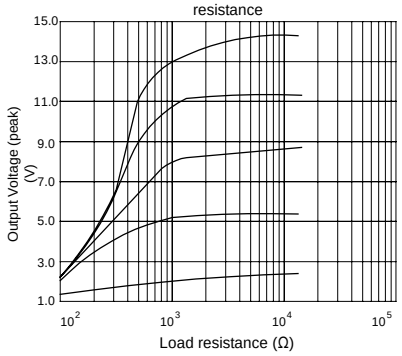


Fig.2 Positive output voltage swing vs Load resistance

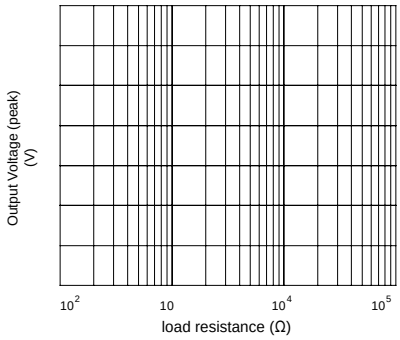


Fig.3 Power bandwith(large signal swing vs frequency)

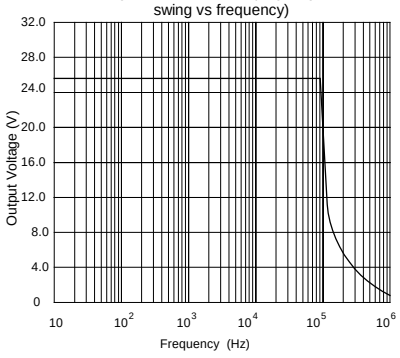


Fig. 4 Burst Noise vs Rs

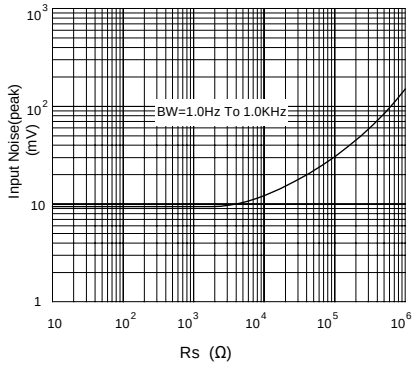


Fig. 5 RMS Noise vs Rs

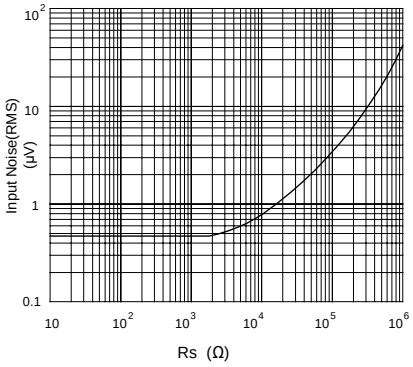


Fig. 6 Output Noise vs Rs

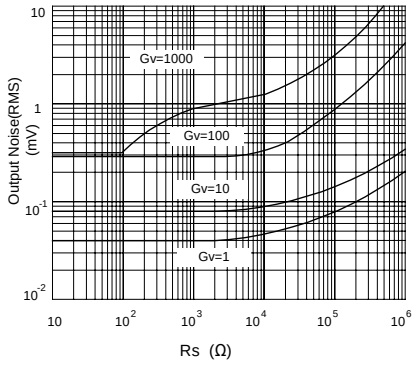


Fig. 7 Spectral Noise Density

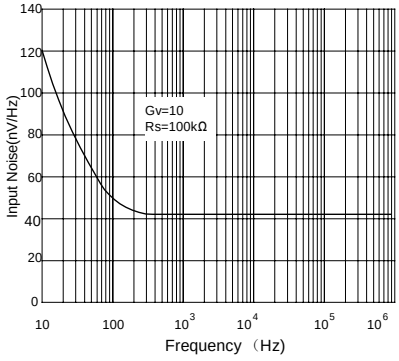


Fig. 8 Open loop frequency response

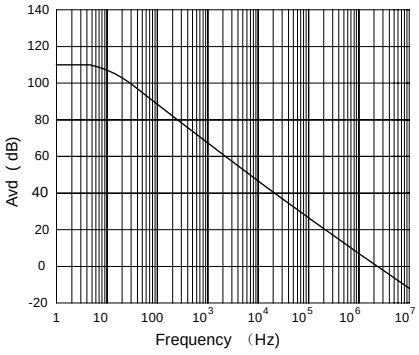
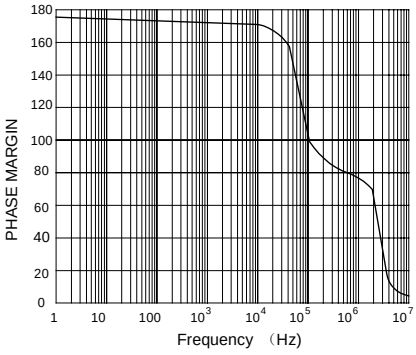
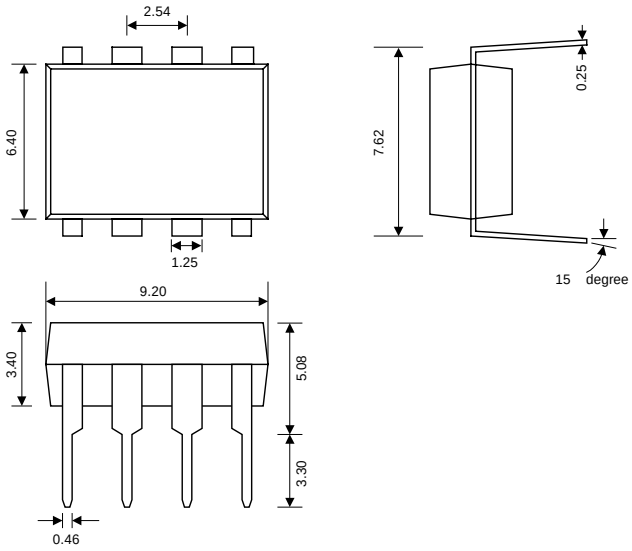


Fig. 9 PHASE MARGIN vs FREQUENCY



PACKAGE DIMENSIONS

8-DIP-P-300



8-SOP-P